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09/811,995	03/19/2001	Matthew J. Adiletta	10559-320001/P9681	9585

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,995	ADILETTA ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-21,23-26,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-21, 23-26, and 28-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 17-21, 23-26, and 28-29 have been considered. Claims 17 and 26 are amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 17 August 2006 and Amendment as received on 17 August 2006.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 August 2006 has been entered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17-21, 23-26, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al., U.S. Patent Number 5,663,012 (herein referred to as Shimizu) in view of David K. Probst's "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors" from Proceedings of the

Twenty-Seventh Annual Hawaii International Conference on System Sciences, 1994 ©1994 IEEE (herein referred to as Probst) and in further view of Harney et al., U.S. Patent Number 4,816,913 (herein referred to as Harney).

6. Referring to claim 17, Shimizu has taught a hardware-based processor comprising:

   a. Each microengine comprising

      i. A context event arbiter (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

      ii. A controller (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

      iii. A control store (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

      iv. Local read and write transfer registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

      v. Local general purpose registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12), and

      vi. An arithmetic logic unit (ALU) (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

   b. Each microengine supporting instructions that perform

      i. An ALU operation on one or two operands (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17),

ii. Deposit a result in a destination register (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17) and

iii. Update ALU condition codes according to the result (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17), and

iv. A local register instruction that loads one or more bytes, specified by a multiple-bit field of the instruction, within a local destination register with a shifted value of another operand (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

7. Shimizu has not taught a multithreaded processor comprising a plurality of microengines. Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page 585, section 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Probst, would have recognized that a multithreaded processor tolerates latencies and increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multithreaded processor of Probst in the device of Shimizu to improve processor utilization. Also, as shown in *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960),

duplicating parts is generally not given patentable weight or would have been obvious improvements.

8. In addition, Shimizu has not taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register. Harney has taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register (Harney column 40, lines 40-50 and Figure 12A). Shimizu has taught that the instructions store the results in a specific location in the destination (Shimizu column 4, line 51 to column 5, line 40), but has not taught the specifics of how these instructions work. In other words, Shimizu has not taught how the instructions specifically designate the destination location, just that the destination location is designated. Harney has taught that the mask designates the destination location where a result is stored (Harney column 40, lines 40-50 and Figure 12A). A person of ordinary skill in the art at the time the invention was made, and as recognized by Harney, would have recognized that the mask of Harney prevents erroneous data from being written into a destination location (Harney column 41, lines 6-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the mask of Harney in the device of Shimizu to prevent erroneous data from entering memory.

9. Referring to claim 18, Shimizu in view of Probst and in further view of Harney has taught wherein the destination register is an absolute transfer register (Shimizu column 4, lines 35-48 and Figure 8).

10. Referring to claim 19, Shimizu in view of Probst and in further view of Harney has taught wherein the destination register is a context-relative transfer register (Shimizu column 4, lines 35-48 and Figure 8).

11. Referring to claim 20, Shimizu in view of Probst and in further view of Harney has taught wherein the destination register is a general-purpose register (Shimizu column 4, lines 35-48 and Figure 8).

12. Referring to claim 21, Shimizu in view of Probst and in further view of Harney has taught wherein the local register instruction comprises the destination register (Shimizu column 4, lines 35-48 and Figure 8).

13. Referring to claim 23, Shimizu in view of Probst and in further view of Harney has taught wherein the mask is 4-bits (Harney column 40, lines 40-50 and Figure 12A).

14. Referring to claim 24, Shimizu in view of Probst and in further view of Harney has taught wherein the mask comprises a set bit indicating a corresponding byte in the local register to be loaded (Harney column 40, lines 40-50 and Figure 12A).

15. Referring to claim 25, Shimizu in view of Probst and in further view of Harney has taught wherein the local register instruction comprises a context relative source register (Shimizu column 4, lines 35-48 and Figure 8).

16. Referring to claim 26, Shimizu has taught an apparatus comprising:

a. In a hardware-based processor, each microengine comprising

i. A context event arbiter (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

ii. A controller (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

iii. A control store (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

iv. Local read and write transfer registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

v. Local general purpose registers (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12), and

vi. An arithmetic logic unit (ALU) (Shimizu column 5, line 41 to column 7, line 32; Figure 11; and Figure 12),

b. Each microengines including a command that causes the ALU to load one or more bytes, specified by a multiple-bit field of the command, within a destination register of a selected microengine with a shifted value of another one or more bytes of a source register (Shimizu column 4, lines 12-34; column 4, line 51 to column 5, line 40; column 10, line 6 to column 11, line 47; Figure 7; Figure 8; Figure 9; Figure 10; Figure 16; and Figure 17).

17. Shimizu has not taught a multithreaded processor comprising a plurality of microengines. Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page 585, section 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Probst, would have recognized that a multithreaded processor tolerates latencies and increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to

incorporate the multithreaded processor of Probst in the device of Shimizu to improve processor utilization. Also, as shown in *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), duplicating parts is generally not given patentable weight or would have been obvious improvements.

18. In addition, Shimizu has not taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register. Harney has taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register (Harney column 40, lines 40-50 and Figure 12A). Shimizu has taught that the instructions store the results in a specific location in the destination (Shimizu column 4, line 51 to column 5, line 40), but has not taught the specifics of how these instructions work. In other words, Shimizu has not taught how the instructions specifically designate the destination location, just that the destination location is designated. Harney has taught that the mask designates the destination location where a result is stored (Harney column 40, lines 40-50 and Figure 12A). A person of ordinary skill in the art at the time the invention was made, and as recognized by Harney, would have recognized that the mask of Harney prevents erroneous data from being written into a destination location (Harney column 41, lines 6-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the mask of Harney in the device of Shimizu to prevent erroneous data from entering memory.

19. Referring to claim 28, Shimizu in view of Probst and in further view of Harney has taught wherein the mask is 4-bits (Harney column 40, lines 40-50 and Figure 12A).

20. Referring to claim 29, Shimizu in view of Probst and in further view of Harney has taught wherein the mask comprises a set bit indicating a corresponding byte in the source register to be loaded (Harney column 40, lines 40-50 and Figure 12A).

21. Claims 17-21, 23-26, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vincent P. Heuring and Harry F. Jordan's Computer Systems Design and Architecture ©1997 (herein referred to as Heuring) in view of David K. Probst's "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors" from Proceedings of the Twenty-Seventh Annual Hawaii International Conference on System Sciences, 1994 ©1994 IEEE (herein referred to as Probst) and in further view of Harney et al., U.S. Patent Number 4,816,913 (herein referred to as Harney).

22. Referring to claim 17, Heuring has taught a hardware-based processor comprising:

a. Each microengine comprising

i. A context event arbiter (Heuring pages 144-145; Figure 4.1; 166-167; and Figure 4.11),

ii. A controller (Heuring pages 144-145; Figure 4.1; 166-167; and Figure 4.11),

iii. A control store (Heuring pages 144-145; Figure 4.1; 153-154; Figure 4.5; 166-167; and Figure 4.11),

iv. Local read and write transfer registers (Heuring pages 144-145; Figure 4.1; 154-156; and Figure 4.6),

v. Local general purpose registers (Heuring pages 144-145; Figure 4.1; Figure 4.3; 153; and Figure 4.4), and

vi. An arithmetic logic unit (ALU) (Heuring pages 144-145; Figure 4.1; Figure 4.3; 157; and Figure 4.7),

b. Each microengine supporting instructions that perform

i. An ALU operation on one or two operands (Heuring pages 157-161),

ii. Deposit a result in a destination register (Heuring pages 157-161) and

iii. Update ALU condition codes according to the result (Heuring pages 38-39 and 286), and

iv. A local register instruction that loads one or more bytes, specified by a multiple-bit field of the instruction, within a local destination register with a shifted value of another operand (Heuring pages 159-161 and Figure 4.8).

23. Heuring has not taught a multithreaded processor comprising a plurality of microengines. Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page 585, section 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Probst, would have recognized that a multithreaded processor tolerates latencies and increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multithreaded processor of Probst in the device of Heuring to improve processor utilization. Also, as shown in *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), duplicating parts is generally not given patentable weight or would have been obvious improvements.

24. In addition, Shimizu has not taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register. Harney has taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register (Harney column 40, lines 40-50 and Figure 12A). Shimizu has taught that the instructions store the results in a specific location in the destination (Shimizu column 4, line 51 to column 5, line 40), but has not taught the specifics of how these instructions work. In other words, Shimizu has not taught how the instructions specifically designate the destination location, just that the destination location is designated. Harney has taught that the mask designates the destination location where a result is stored (Harney column 40, lines 40-50 and Figure 12A). A person of ordinary skill in the art at the time the invention was made, and as recognized by Harney, would have recognized that the mask of Harney prevents erroneous data from being written into a destination location (Harney column 41, lines 6-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the mask of Harney in the device of Shimizu to prevent erroneous data from entering memory.

25. Referring to claim 18, Heuring in view of Probst and in further view of Harney has taught wherein the destination register is an absolute transfer register (Heuring pages 69-71, Table 2.8).

26. Referring to claim 19, Heuring in view of Probst and in further view of Harney has taught wherein the destination register is a context-relative transfer register (Heuring pages 69-71, Table 2.8).

27. Referring to claim 20, Heuring in view of Probst and in further view of Harney has taught wherein the destination register is a general-purpose register (Heuring pages 157-161).

28. Referring to claim 21, Heuring in view of Probst and in further view of Harney has taught wherein the local register instruction comprises the destination register (Heuring pages 157-161).

29. Referring to claim 23, Heuring in view of Probst and in further view of Harney has taught wherein the mask is 4-bits (Harney column 41, lines 6-7).

30. Referring to claim 24, Heuring in view of Probst and in further view of Harney has taught wherein the mask comprises a set bit indicating a corresponding byte in the local register to be loaded (Harney column 41, lines 6-7).

31. Referring to claim 25, Heuring has taught wherein the local register instruction comprises a context relative source register (Heuring pages 69-71, Table 2.8).

32. Referring to claim 26, Heuring has taught an apparatus comprising:

a. In a hardware-based processor, each microengine comprising

i. A context event arbiter (Heuring pages 144-145; Figure 4.1; 166-167; and Figure 4.11),

ii. A controller (Heuring pages 144-145; Figure 4.1; 166-167; and Figure 4.11),

iii. A control store (Heuring pages 144-145; Figure 4.1; 153-154; Figure 4.5; 166-167; and Figure 4.11),

iv. Local read and write transfer registers (Heuring pages 144-145; Figure 4.1; 154-156; and Figure 4.6),

v. Local general purpose registers (Heuring pages 144-145; Figure 4.1; Figure 4.3; 153; and Figure 4.4), and

vi. An arithmetic logic unit (ALU) (Heuring pages 144-145; Figure 4.1; Figure 4.3; 157; and Figure 4.7),

b. Each microengines including a command that causes the ALU to load one or more bytes, specified by a multiple-bit field of the command, within a destination register of a selected microengine with a shifted value of another one or more bytes of a source register (Heuring pages 159-161 and Figure 4.8),

33. Heuring has not taught a multithreaded processor comprising a plurality of microengines. Probst has taught a multithreaded processor comprising a plurality of microengines (Probst page 585, section 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Probst, would have recognized that a multithreaded processor tolerates latencies and increases processor utilization (Probst page 585, section 2, paragraph 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multithreaded processor of Probst in the device of Heuring to improve processor utilization. Also, as shown in *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), duplicating parts is generally not given patentable weight or would have been obvious improvements.

34. In addition, Shimizu has not taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register. Harney has taught the field representing a mask in which each bit of the mask identifies a different byte of the destination register (Harney column 40, lines 40-50 and Figure 12A). Shimizu has taught that the instructions store the results in a specific location in the destination (Shimizu column 4, line 51 to column 5, line 40), but has not taught the specifics of how these instructions work. In other

words, Shimizu has not taught how the instructions specifically designate the destination location, just that the destination location is designated. Harney has taught that the mask designates the destination location where a result is stored (Harney column 40, lines 40-50 and Figure 12A). A person of ordinary skill in the art at the time the invention was made, and as recognized by Harney, would have recognized that the mask of Harney prevents erroneous data from being written into a destination location (Harney column 41, lines 6-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the mask of Harney in the device of Shimizu to prevent erroneous data from entering memory.

35. Referring to claim 28, Heuring in view of Probst and in further view of Harney has taught wherein the mask is 4-bits (Harney column 40, lines 40-50 and Figure 12A).

36. Referring to claim 29, Heuring in view of Probst and in further view of Harney has taught wherein the mask comprises a set bit indicating a corresponding byte in the source register to be loaded (Harney column 40, lines 40-50 and Figure 12A).

Response to Arguments

37. Applicant's arguments with respect to claims 17-21, 23-26, and 28-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Burke et al., U.S. Patent Number 4,808,988, has taught a mask that indicates the destination bit positions of results in an accumulation register.

b. Patti et al., U.S. Patent Number 5,189,636, has taught a mask indicating the destination position of results in memory.

c. Divivier et al., U.S. Patent Number 5,980,564, has taught a mask indicating the destination of fetched instructions in prefetch buffers.

d. Redford, U.S. Patent Number 5,946,222, has taught a masked add byte operation that shifts and loads data into registers.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJL
Aimee J. Li
27 October 2006